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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,400	UHLER, G. MICHAEL	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 18 -23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

3. Claim 18 is directed to a bit clear instruction. This instruction is at best functional descriptive data. The claimed instruction does not fit in any of the statutory categories of invention (process, machine, manufacture, or composition of matter). Claim 18 provides (in the preamble) intended execution on a microprocessor having privileged control register under the condition of executing on the microprocessor when the microprocessor receives and interrupt and when the microprocessor is in a privileged state. The claim also provides a wherein clause that indicates wherein the plurality of bits within the privileged control register that are specified by said bit mask are cleared atomically. However each of these limitations are conditions and intended use. The claim is not to an apparatus or process or manufacture or composition of matter. Even if the intended steps (such as in a method or process claim) were considered, no physical transformation of matter is produced. Also no tangible result is produced [the clearing of bits is not tangible]. As to whether the a useful result is produced since only a clearing of non-specific bits in a control register where the use of the information (cleared bits) in some operation of the system or external to the system is not specified in the claims then the claims is non-statutory. Claims 19 is dependent on claim 18 and provides for a

interrupt mask field. This mask field does not limit the invention to any of the statutory classes of invention and does not provide any additional steps or means that would result in any concrete, useful and tangible result and consequently claim 19 also is non statutory.

4. Claims 20 is directed to a computer program product comprising computer program code embodied in a computer useable medium. The computer useable medium is disclosed in one embodiment as a carrier wave (see page 41 of the instant application). The program code embodied on a carrier was does not fit in any of the statutory classes of invention (process, machine, manufacture, composition of matter. The embodying of information including a computer program product on a carrier wave is not embodied in a manner so as to be tangible (the computer readable medium must be physical which permits functionality to be realized with the computer and effect a useful, concrete and tangible result, not a signal). Consequently Claim 20 is directed to non-statutory subject matter (See In re Lowry USPQ2d 1031 (Fed. Cir. 1994)). Claims 21-22 depend from claim 20 and are rejected for the same reasons. Claim 23 is directed to a data signal embodied in a transmission medium. The embodying of data signal in a transmission medium is not embodied in a manner so as to be tangible (the transmission medium is not a physical medium which permits functionality to be realized with the computer and effect a useful, concrete and tangible result, transmission medium). Consequently, Claim 23 is directed to non-statutory subject matter (See In re Lowry USPQ2d 1031 (Fed. Cir. 1994).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1,2,4,5 and 18-23, are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren (patent No. 5,9,805,918) in view of and iAPX88 Book (book published by Intel).

7. Blomgren taught the invention substantially as claimed including a data processing ("DP") system comprising: (as per claim 1,18,20,22,23)

8. Microprocessor (CPU) (e.g., see col. 3, lines 22-30) having a control register (EFLAGS register) (e.g., see col. 5, line 35-col. 6, line 44) that is atomically modifiable by a privileged (kernel instruction) [(e.g., see col. 6, lines 12-25)[The EFLAGS register has control bits that are set or cleared only by complex or infrequently used CISC instructions such as privileged instructions]; the control register having bit fields (e.g., see col. 6, line 51-col. 6, line 10) comprising a core (CPU)(e.g., see col. 3, lines 22-30).

9. Blomgren did not expressly detail (claim 1,20) that the core was for receiving a privileged instruction. Blomgren however taught the CPU operating in CISC, RISC and emulation mode for executing instructions (e.g., see col. 3, lines 31-41). Blomgren also taught the privileged instructions were emulated and the emulated instructions modified the control bits in the CISC EFLAGS register (e.g., see col. 6, lines 12-20). Therefore it would have been obvious to one of ordinary skill that the core in the Blomgren system received the privileged instructions that were emulated. As to the atomically modifying

the control register the control bits were modified by privileged instructions in the Blomgren system as discussed above. The status bits such as the interrupt enabled flag is a flag that was used by user mode programs to process interrupts and therefore since these bits were "seen by" the user mode programs then their modification would have been atomic (e.g., see col. 8,lines 3-7 and col. 14, lines 46-63 and col. 9, lines 39-60).

10. Claim 1,18,20,23 also comprises clauses claiming said bit mask is used to atomically set or clear (claims 1,20) or clear (claims 18,22,23) the bit field in a control register; and wherein the bit fields in the control register are modified atomically by the privileged instruction. As to these limitations Blomgren taught the modifying of the bits in the EFLAGS register using the privileged instruction (e.g., see col. 6, lines 12-20). Since bits inherently store either one or zeros the modification of bit fields would have been recognized by one of ordinary skill to include setting or clearing the bit fields. On the other hand, IAPX taught a CLI instruction that cleared the IF bit from the flags register (e.g., see page 2-64).

11. It would have been obvious to one of ordinary skill I the DP art to combine the teachings of Blomgren and IAPX. Both reference were directed toward the operations of the x86 processors and the modifying of the bits in the control register (e.g., see col. 5, line 65-col. 6 line 28). Blomgren. did not specify the particular instructions that modified the control register. Therefore one of ordinary skill would have been motivated to incorporate the teaching of IAPX to fully implement the modification of the EFLAGS register in the combined system (e.g., see page 2-16 of IAPX).

12. Blomgren did not specify (claims 1,18,20,23) contents of the modifying instruction. Theses claim limitations merely provide a data structure and intended use for the bits in the data structure and do not provide any change in the operation of the system. Further, the claim limitations to the content of the instruction are labels to bits of an instruction where the functions of indicating the privileged instruction as a privileged instruction, and indication that the flags register was to be modified and specifying a location of a mask for masking the bits of the flags register would have been required of the instruction in the Blomgren system that modified the EFLAGS control bits. [Blomgren limited the modification of the control bits to only certain instructions so an indication of the type of instruction would have been required (e.g., see col. 6, lines 12-28); Bloomgren taught a plurality of registers (e.g., see figs. 1,2) and therefore the indication that the register to be modified was the control register was required and since a plurality of control bits were in the EFLAGS register (e.g., see fig. 3) then a particular mask for the particular flag would have to have been accessed to indication of the mask to be used would have had to had been indicated by the instruction. The use of registers for masking was well known in the art at the time of the claimed invention. One of ordinary skill would have been motivated to use registers to perform the masking at least because registers would have been quickly accessible by the system].[These requirements for the Blomgren instructions would have been required whether or not the instruction was encoded as separate fields or as a single field with different values of the field decoded to indicate the instruction requirements (discussed above).

Therefore the operation of the system in response to decoding the instruction in Blomgren and the instruction in the claims would have been the same].

13. As per claim 2, Blomgren taught the control register was not accessible when the microprocessor is executing unprivileged instructions (e.g.. see col. 6, lines 1-20).

14. As per claim 19, IAPX taught a control register comprising a status register having a plurality of bit fields including the bits (e.g., see flags register on page 2-2) comprising a interrupt mask field (IF) (e.g., see page 2-16, col. 2).

15. As per claim 4, 5, 21, IAPX taught the CLI instruction allows maskable interrupts and STI instruction that enables external interrupts and therefore during operation of the system receives interrupts (e.g., see col. 2-16).Blomgren also taught control bit that enables interrupts (e.g, see col. 6, lines 1-10). Consequently one of ordinary skill would have been motivated to execute the STI or CLI instruction when an interrupt occurred at least to take advantage of the control of whether the interrupt was to be enabled or not.

16. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over over Blomgren (patent No. 5,9,805,918) in view of and iAPX88 Book (book published by Intel) as applied to claims 1-2 above, and further in view of in view of Bhandai (patent No. 6,532,533) or Mann (patent No. 6,560,698).

17. As per claim 3, Bhandai taught the register is directly modified without requiring the contents of the register to first be moved to a general purpose (i.e., privileged) register (e.g., see col. 2, lines 16-35 and col. 5, lines 16-52). This allows the modifying of the register without performing read modify write that eliminates that problems associated with performing read modify write. As to the combining the teachings of

Bhandai, and Blomgren and IAPX, one of ordinary skill would have been motivated to use the Bhandai method of masking of bits of register for the control register of Blomgren and IAPX (e.g., see col. 8,lines 3-7 and col. 14, lines 46-63 of Blomgren and page 2-16 of IAPX) at least to provide a more direct method for modifying the control register that took less time.

18. Alternatively Mann taught (e.g., see fig. 4 and col. 7, line 4-col. 8, line 44) a register is directly modified by an resource change registers each of the resource change registers is tied to a specific bit in a summary register where the a bit set in the summary register controls whether an interrupt is triggered. This provided for the modification of the summary register without moving the first register (summary register to a general purpose register (e.g., see fig. 4 of Mann). As to the combining the teachings of Mann and Blomgren and IAPX one of ordinary skill woiuld have been motivated to use the Mann method of masking bits of a register for the control register of Blomgren and IAPX (e.g., see col. 8, lines 3-7 and col. 14, lines 46-63 of Blomgren and page 2-16 of IAPX)) at least to provide a more direct method for modifying the control register that took less time.

19. Claims 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over over Blomgren (patent No. 5,9,805,918) in view of and iAPX88 Book (book published by Intel). as applied to claims 1-2,4-5 above, and further in view of in view of Col (patent No. 5,887, 175).

20. As per claim 6,7, Col taught the instruction that sets bit fields in the control register in the control register corresponding to the bits in the bit mask(e.g., see col. 9,

lines 12-62). As to the clearing of the control register bits. IAPX taught CLI instruction (e.g., see page 2-16, col. 2). As to the combination of Blomgren and IAPX and Col, one of ordinary skill would have been motivated to utilize the Col method of modifying the control bits (as taught for the STI instruction) for the CLI instruction at least because the combined system would have comprised the means to perform the masking of the same bit (STI and CLI modify the same bit) that controlled interrupts and doing so would take advantage of the means provided in the Col reference to efficiently mask the (IF) bit in the control register (e.g., see col. 6 lines 1-54 of Col).

21. As to claim 8, Col taught a second register comprising a general purpose register (register containing the MASK operand field) (e.g., see col. 9, lines 12-46).

22. As to claim 9,10 IAPX taught a field for specifying whether the bits fields in the control register are to be set or cleared (e.g., see page 63, under processor control). Since the STI and CLI instruction set or cleared specific bits of a register, one of ordinary skill would have been motivated to mask the bits of the register. Therefore since the Col reference taught a register storing a mask and an efficient manner to mask the bits of the control register one of ordinary skill would have been motivated to use the Col teachings of specifying bits a control register using the mask bits (e.g., see col. 9, lines 12-46 of Col.).

23. As per claim 11, Blomgren. taught the modifying (that comprises setting or clearing) of the bit of the plurality of bits using the privileged instruction its corresponding interrupt is disabled)[The EFLAGS register has control bits that are set or cleared only by complex or infrequently used CISC instructions such as privileged

instructions]; the control register having bit fields (e.g., see col. 6, line 51-col. 6, line 10) comprising a core (CPU)(e.g., see col. 3, lines 22-30).

24. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren (patent No. 5,9805,918) in view of Col (patent No. 5,887, 175) and iAPX88 Book (book published by Intel).

25. As per claim 12, Blomgren taught atomically modifying bits within a privileged control register of a microprocessor by providing an instruction which instruction the microprocessor to atomically modify specified ones of the bits)[The EFLAGS register has control bits that are set or cleared only by complex or infrequently used CISC instructions such as privileged instructions (e.g., see col. 8, lines 3-8)]; the control register having bit fields (e.g., see col. 6, line 51-col. 6, line 10) comprising a core (CPU)(e.g., see col. 3, lines 22-30). The status bits such as the interrupt enabled flag is a flag that was used by user mode programs to process interrupts and therefore since these bits were "seen by" the user mode programs then their modification would have been atomic (e.g., see col. 8,lines 3-7 and col. 14, lines 46-63 and col. 9, lines 39-60).

26. Claim 12 provides for the clearing of specified bits. As to these limitations Blomgren taught the modifying of the bits in the EFLAGS register using the privileged instruction (e.g., see col. 6, lines 12-20). Since bits inherently store either one or zeros the modification of bit fields would have been recognized by one of ordinary skill to include setting or clearing the bit fields.

27. Blomgren did not expressly (claim 12) detail a register specifying which of the particular ones of the bits to be cleared. Col. however taught (e.g., see col. 9, lines 19-

46) a register (910) that contains two operands (912,914) that are used to provide operands to microinstruction including the Mask that specified which of particular ones of the bits are to be modified (which in the STI instruction one the bit is set and the other bits in the Eflags register are not modified). Since the Col. processor comprises a register to indicate the bit to be modified in an instruction that sets the a bit in the Eflags one of ordinary skill would have been motivated to utilized the same register or a similar register to indicate the bits to clear (when a clear instruction in the instruction set is perfomed) in the Elfags register at least to take advantage of the means already part of the system that determines which bit to modify in the Eflags register. As to the modifying of the bits of the Eflags register happened upon receipt of an interrupt Col. taught the STI instruction is accessed from a ROM that contains instructions that are used by exception handler 952 and floating point exception handler (954) (e.g., see col. 9, lines 4-11). Therefore it would have been obvious to one of ordinary skill that upon receipt of an interrupt and exception handler would have accessed the instruction register 910 to provide the mask for the IF bit of the Eflags register for modification thereof for setting or clearing the bits depending on system conditions and the type of interrupt for allowing interrupts or masking interrupts. This operation would have been atomic as detailed above.

28. As to the combination of Blomgren and Col, one of ordinary skill would have been motivated to utilize the Col method of modifying the control bits (as taught for the STI instruction) for the instruction that modified control bits at least because the combined system would have comprised the means to perform the masking of the same

bit that controlled interrupts and doing so would take advantage of the means provided in the Col reference to efficiently mask the interrupt enable bit in the control register (e.g., see col. 6 lines 1-54 of Col).

29.

30. Col did not expressly detail that the instruction that modified the bit of the Eflags register cleared the bit. However IAPX taught the STI instruction that set the IF flag (e.g,. see page 2-16 col. 1) IAPX also taught the CLI instruction that cleared the interrupt enable flag in the 8088 microprocessor (e.g,. see pages 2-16,2-2,2-3 and 2-64).

31. It would have been obvious to one of ordinary skill I the DP art to combine the teachings of Col. and IAPX. Both reference were directed toward the operations of the x86 processors and the modifying of the bits in the control register. Col. did not specify the entire instruction set that operated on the flags register. Col. however taught a flaw in the architecture when executing an instruction to modify the bits of the control register and then an interrupt occurred that would make the processor hang and processing mask flag transitions to prevent hanging (e.g., see col. 3, lines 18-34 and col. 4, lines 6-46). Therefore one of ordinary skill would have been motivated to incorporate the IAPX teachings of the rest of the instructions in the x86 instruction set that operated on the control registers at least to fully implement the functionality of the flags in an implementation of the x86 processor for processing interrupts and to apply the Col teachings to any instructions that modified the control register to prevent hanging of the system (e.g., page 2-16 of IAPX and col. 3, lines 18-34).

32. As per claim 13,14 IAPX taught the bits of the of the flags register indicate which of the plurality of interrupts have been received (e.g., see page 2-16 and 2-17) where the flags (IF and TF) indicate whether indicate external interrupts are enabled or disabled consequently by checking the IF bit it can determined the type of interrupt that was allowed to be enabled.

33. As per claim 15, IAPX taught a control register comprising a status register having a plurality of bit fields including the bits (e.g., see flags register on page 2-2).

34. As per claim 16 Blomgren did not specify contents of the modifying instruction. Theses limitations merely provided a data structure and intended use for the bits in the data structure and do not provide any change in the operation of the system. Further the limitations to the content of the instruction are labels to bits of an instruction where the functions of indicating the privileged instruction as a privileged instruction; and indication that the flags register was to be modified and specifying a location of a mask for masking the bits of the flags register would have been required of the instruction in the Blomgren system that modified the EFLAGS control bits. [Blomgren limited the modification of the control bits to only certain instruction so an indication of the type of instruction would have been required (e.g., see col. 6, lines 12-28); Bloomgren taught a plurality of registers (e.g., see figs. 1,2) and therefore the indication that the register to be modified was the control register was required and since a plurality of control bits were in the EFLAGS register (e.g., see fig. 3) then a particular mask for the particular flag would have to have been accessed to indication of the mask to be used would have had to had been indicated by the instruction. The use of registers for masking was

well known in the art at the time of the claimed invention. One of ordinary skill would have been motivated to use registers to perform the masking at least because registers would have been quickly accessible by the system].[These requirements would have been required whether or not the instruction was encoded as separate fields or as a single field with different values of the field was decoded to indicate the instruction requirements discussed above an the operation of the system in response to decoding the instruction in Blomgren and the instruction in the claims would have been the same].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER